UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/692,852	10/20/2000	Andrew R. Osborn	65,135-008	6250

27305 7590 12/16/2004

HOWARD & HOWARD ATTORNEYS, P.C.
THE PINEHURST OFFICE CENTER, SUITE #101
39400 WOODWARD AVENUE
BLOOMFIELD HILLS, MI 48304-5151

EXAMINER	
STRANGE, AARON N	
ART UNIT	**PAPER NUMBER**
2153	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/692,852	OSBORN ET AL.	
	Examiner	Art Unit	
	Aaron Strange	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03292002, 01032001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 18 is objected to because of the following informalities: There appears to be a typographical error, "sent form a sending processor", in line 2. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 9-13, and 48-67 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

4. With regard to claim 9,48 and 58, the specification fails to disclose how creating a virtual memory map of each of the codes may be done "such that the first and second processors can address and forward processed information to each of the indexed processors within the system". The specification, in Page 10, Line 24 to Page 11, Line 1, states that "The virtual memory maps 58, 60 are essentially a means for the processors 40, 42 to be able to address each other processor of node 1-6 within the

system 30." It is unclear how the virtual memory maps provide a means for processors to address each other.

5. With regard to claim 18, the specification fails to provide support for "limiting the number of times that the processed information can be sent from a sending processor". The claim language does not appear in the specification, and no mechanism is described which would limit the number of times that the processed information can be sent from a sending processor.

6. All claims not individually rejected are rejected by virtue of their dependency form the above claims.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 8-18, 27-35, 40,43,44, and 67 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. With regard to claim 8, it is unclear if "indexing the processors to define a different code for each of the processors for differentiating the processors " is supposed to redefine the step of "indexing the first and second processors" defined in claim 1 or add an additional step to indexing the processors. If Applicant intended for an additional

step to be added, the Examiner recommends that the claim be amended to recite "wherein the step of indexing the first and second processors further comprises defining a different code for each..." or a similar recitation.

10. With regard to claim 8, it is unclear what the "code" is. The term "code" is not defined by the claim or the specification and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The specification only defines the term using the claim language, and the only examples state that it has the same value as the destination address. It is unclear how the code differs from the destination address.

11. With regard to claims 10 and 30, the term "indicative" renders the claim indefinite. The term "indicative" is not defined by the claim or the specification and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The specification only defines the term using the claim language, and it is unclear how the address may be "indicative of the code of the addressed processor".

12. With regard to claims 12 and 32, it is unclear if "assigning a memory address onto the processed information indicative of the memory location of the addressed processor" is supposed to redefine the "step of addressing the processed information" defined in claim 10 or add an additional step to addressing the processed information. If Applicant intended for an additional step to be added, the Examiner recommends that

the claim be amended to recite "wherein the step of addressing the processed information further comprises assigning a memory address..." or a similar recitation.

13. With regard to claims 12 and 32, the term "indicative" renders the claim indefinite. The term "indicative" is not defined by the claim or the specification and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The specification only defines the term using the claim language, and it is unclear how the memory address may be "indicative of the memory location of the addressed processor".

14. With further regard to claims 12 and 32, it is unclear what a "memory address" is. The term "memory address" is not defined by the claim or the specification and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It is unclear what the memory address is supposed to represent. The specification only defines the term using the claim language, and the only examples state that it has the same value as the destination address. It is unclear how the memory address differs from the destination address.

15. With regard to claim 27, it is unclear if the step of defining "a different code for each of said processors for differentiating said processors" is in addition to or a more specific definition of defining "different destination addresses for each of said processors" defined in claim 19. If Applicant intended for an additional step to be added,

the Examiner recommends that the claim be amended to recite "wherein said indexer further defines a different code..." or a similar recitation.

16. With regard to claim 27, it is unclear what the "code" is. The term "code" is not defined by the claim or the specification and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The specification only defines the term using the claim language, and the only examples state that it has the same value as the destination address. It is unclear how the code differs from the destination address.

17. With regard to claim 39, the limitation "at least on destination pointer for sending said processed information" is unclear. It is unclear how the destination pointer is capable of sending processed information, since it only points to a location in memory.

18. With regard to claim 39, the limitation "wherein said pair of pointers includes a next task pointer...and at least one data destination pointer" is unclear. The limitation "said pair" limits the number of pointers to two, but a next pointer and "at least one" destination pointer may exceed two.

19. With regard to claim 39, the limitation "wherein said at least one destination pointer includes a plurality of data destination pointers" is unclear. The limitation "said

pair", recited in claim 39, limits the number of pointers to two, but a next pointer and "A plurality of destination pointers" exceeds two.

20. Claims 40 and 67 recites the limitation "said at least one data destination pointer" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

21. With regard to claim 43, the functionality of the counter is unclear. "said processed information" presumably is referring to the processed information defined in claim 19. The processed information in claim 19 is only sent a single time. It is unclear if the same processed information will be sent numerous times or different processed information is being sent and counted, as would be the case if the system were reporting dynamic test results. The specification provides no further explanation beyond the claim language, so the scope of the claim cannot be determined.

22. All claims not individually rejected are rejected by virtue of their dependency form the above claims.

Claim Rejections - 35 USC § 102

23. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

24. Claims 1,2,3,5,6,8,19,20,21,27,7,37, and 47 rejected under 35 U.S.C. 102(b) as being anticipated by Antonov (US 5,884,046).

25. With regard to claim 1, Antonov discloses a method of communicating across a distributed multiprocessing system having a first processor and a second processor (workstations) (Fig 2, 13), the first and second processors being connected to a central signal routing hub (Fig 1, 17) by first and second communication links, respectively, said method comprising the steps of: processing information within at least one of the first and second processors (generate message); addressing the processed information using at least one of the destination addresses (specify recipient); transmitting the processed information from at least one of the first and second processors across at least one of the communication links toward the hub, thereby defining at least one sending processor (Col 5, Lines 49-53); receiving the processed information along with the at least one destination address within the hub (Col 5, Lines 54-55); identifying the destination address for the transmitted processed information within the hub; and sending the processed information without modification over at least one of the communication links to at least one of the first and second processors associated with the at least one destination address, thereby defining at least one addressed processor (inter-workstation message is received and routed to recipient) (Col 5, Lines 55-65).

Antonov fails to specifically recite indexing the first and second processors to define different destination addresses for each of the processors. However, in order for the processors to communicate with each other, they must be assigned a destination

address in order for messages to be properly routed. Therefore, Antonov further discloses indexing the fist and second processors to define different destination addresses for each of the processors, since the processors are able to identify and communicate with other processors (Col 5, Lines 49-51).

26. With regard to claim 2, Antonov further discloses that the step of processing information is further defined as creating data (creating a message) within at least one of the first and second processors (Col 5, Lines 49-53).

27. With regard to claim 3, Antonov further discloses that the step of processing information is further defined as compiling the data (creating a packet with the message and addressing information) within at least one of the first and second processors (Col 5, Lines 49-53).

28. With regard to claim 5, Antonov further discloses that the step of transmitting the processed information is further defined as transmitting the processed information across at least one of the communication links in only one direction from at least one of the first and second processors to the hub to define a send-only system (The packet is sent directly to the hub) (Col 5, Lines 49-55 and Fig 2).

29. With regard to claim 6, Antonov further discloses that the step of sending the processed information without modification is further defined as sending the processed

information over at least one of the communication links in only one direction from the hub to at least one of the first and second processors to the hub to further define the send-only system (The packet is forwarded to the recipient by the hub) (Col 5, Lines 54-65).

30. With regard to claim 8, as discussed regarding claim 1, Antonov fails to specifically recite indexing the first and second processors to define a different code for each of the processors for differentiating the processors. However, in order for the processors to communicate with each other, they must be differentiated in order for messages to be routed to the intended recipient. Therefore, Antonov further discloses indexing the fist and second processors to define a different code for each of the processors for differentiating the processors, since the processors are able to identify and communicate with other processors (Col 5, Lines 49-51).

31. With regard to claim 19, Antonov discloses a distributed multiprocessing system comprising: a first processor for processing information at a first station and for assigning a first address to a first processed information, a second processor for processing information at a second station and for assigning a second address to a second processed information (workstations) (Fig 2, 13), a central signal routing hub (Fig 1, 17), a first communication link interconnecting said first processor and said hub for transmitting said first processed information between said first processor and said hub (Fig 2, 11C); a second communication link interconnecting said second processor

and said hub for transmitting said second processed information between said second processor and said hub (Fig 2, 11), said central routing hub including a sorter for receiving at least one of said first and second processed information from at least one of said first and second processors, thereby defining at least one sending processor (Message is received at a processing node) (Col 5, Lines 54-55), and for associating a destination of at least one of said first and second addresses of said first and second processed information, respectively, with at least one of said destination addresses, and for sending at least one of said first and second processed information without modification over at least one of said communication link to at least one of said first and second processors associated with said destination address, thereby defining at least one addressed processor (message is routed to the recipient) (Col 5, Lines 55-65).

Antonov fails to specifically recite an indexer connected to said routing hub for indexing said first and second processors to define different destination addresses for each of said processors. However, in order for the processors to communicate with each other, they must be assigned a destination address in order for messages to be properly routed. Since the processors are able to identify and communicate with other processors (Col 5, Lines 49-51), Antonov further discloses an indexer indexing the first and second processors to define different destination addresses for each of the processors. The indexer must be connected to the hub since the messages are routed by the hub and it must have the appropriate addresses in order to properly route the messages.

32. With regard to claims 20 and 21, Antonov further discloses that said first and second communications links each include incoming and outgoing transmission lines (Fig 1, 11 and 11C). Since the workstations can communicate in both directions in order to request and send data to each other, incoming and outgoing transmission lines are present (Col 6, Lines 40-50).

33. With regard to claim 27, as discussed regarding claim 1, Antonov fails to specifically recite an indexer connected to said routing hub which defines a different code for each of said processors for differentiating said processors. However, in order for the processors to communicate with each other, they must be differentiated in order for messages to be routed to the intended recipient. Therefore, Antonov further discloses that the indexer defines a different code for each of said processors for differentiating said processors, since the processors are able to identify and communicate with other processors (Col 5, Lines 49-51).

34. With regard to claims 36 and 37, Antonov further discloses that each of first and second processors include at least one task and executable code for processing information defined by each of said tasks (Col 5, Line 46 to Col 6, Line 51). The first and second processors generate and receive messages as well as respond to them with any data that may have been requested. Executable instructions are necessary for the processors to perform these tasks.

35. With regard to claim 47, Antonov further discloses that said sorter includes hardware for determining destination addresses of said addressed processors (Col 6, Lines 8-16).

Claim Rejections - 35 USC § 103

36. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

37. Claims 14-17, 33-35, 41,42, 45, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Antonov (US 5,884,046).

38. With regard to claims 14-17, and 33-35, while the system disclosed by Antonov shows substantial features of the claimed invention (discussed above), it fails to specifically disclose connecting an additional hub, having third and fourth processors, by a hub link and reconfiguring the system so that the third and fourth processors may communicate with the first and second processors.

However, Antonov discloses that the invention should be scalable to allow for the addition of mode nodes, and further states that the type of interconnect is not limited to any specific type (Col 4, Lines 32-33). Connecting another hub with additional processors and reconfiguring the system to notify the newly connected processors and

the current processors about each other would have been an advantageous way to scale the system since it would have allowed additional processors to be added to the system and communicate with the processors already present, and would have allowed independent implementations of the invention to be combined into a single network. This would allow the system to be easily scaled by connecting additional hubs as needed.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect another hub with additional processors and reconfigure the system to notify the newly connected processors and the current processors about each other. This would have allowed the system to be scaled by adding additional hubs and processors as needed.

39. With regard to claims 41 and 42, Antonov further discloses a chipset interconnected between each of said incoming and outgoing communication links and said corresponding processors for creating a virtually transparent connection there between and a buffer disposed between each of said processors and said chipsets. Antonov discloses that workstations are connected to the processing nodes via network links (Col 5, Lines 6-7). All network links require a chipset that prepares packets for transmission over them, as well as a buffer for holding data prior to packaging the data into a packet for transmission.

40. With regard to claims 45 and 46, the system disclosed by Antonov shows substantial features of the claimed invention (discussed above), including a host computer connected to one of said first and second processors, having a digital signal processing card. All of the workstations disclosed by Antonov are host computers connected to their respective processor and connected to the processing nodes of the central hub via a network link (Col 5, Lines 6-7). The workstations disclosed by Antonov must have a digital signal processing card since they communicate via a digital network, which requires a network card capable of processing digital signals to access. Antonov fails to specifically disclose said host computer having a digital signal processing card and at least one peripheral device.

The Examiner takes official notice that peripheral devices such as monitors and keyboards are old and well known in the art and are components of virtually every workstation computer. These devices are well known and advantageous since they allow users to interact with a workstation using a monitor and keyboard.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made provide peripherals such as a monitor and keyboard to allow users to interact with the workstations in the system disclosed by Antonov.

41. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Antonov (US 5,884,046) in view of Kisor (US 6,098,091).

42. With regard to claim 4, while the system disclosed by Antonov shows substantial features of the claimed invention (discussed above), it fails to specifically disclose that the step of transmitting the processed information is further defined as transmitting data along with executable code from the sending processor to the addressed processor.

Kisor discloses a sytem where a computer can assign tasks to idle remote computers, which can work on the task and return completed results. This allows the results to be calculated much faster since a plurality of computers can work on the data in parallel. Kisor discloses that data and instructions for competing the assigned task are sent to the remote computer when the task is assigned (Col 6, Lines 31-35). This would have been an advantageous addition to the system disclosed by Antonov since it would have allowed workstations to assign tasks to other workstations by sending data and executable instructions to them. This would have allowed calculations to be performed much more quickly.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to allow transmission of data along with executable instructions between the processors since it would have allowed one processor to work on data for another processor to speed up the completion of a task.

43. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Antonov (US 5,884,046) in view of Spurgeon.

44. The Examiner would like to note that the Spurgeon reference is an excerpt from a book, obtained through Safari Tech Books Online. Only the relevant cited sections have been included with the Office action, since the entire reference is several hundred pages.

45. With regard to claims 22-24, while the system disclosed by Antonov shows substantial features of the claimed invention (discussed above), it fails to specifically disclose that the incoming and outgoing transmission lines transmit signals in only one direction, defining a send-only system or that the links are unidirectional fiber. Antonov does disclose that the workstations communicate with the hub via a Local Area Network (Col 5, Lines 46-49).

Spurgeon discloses the use of unidirectional fiber optic cables for implementing an Ethernet network. Ethernet is a well-known and very common type of Local Area Network. The 10BASE-FL standard for Ethernet requires the use of two unidirectional fiber links for transmitting and receiving data. Optical fibers are advantageous since they are completely electrically isolated, and are immune to electrical interference (Spurgeon, Section 8.3.1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use unidirectional fiber links for the incoming and outgoing transmission lines to define a send only system. This would have allowed full duplex communication across electrically isolated connections, allowing the system to be used in areas with large amounts of electrical noise, such as a manufacturing environment.

46. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Antonov (US 5,884,046) in view of Eidson (US 6,125,420).

47. With regard to claims 25 and 26, while the system disclosed by Antonov shows substantial features of the claimed invention (discussed above), it fails to specifically disclose at least one actuator connected to at least one of said first and second processors, respectively, for performing a testing operation during an operation of said system or that said actuator is a servo-hydraulic actuator.

Eidson discloses the use of actuators in a distributed control system to implement control functions for controlling devices connected to the system (Col 4, Lines 56-67). Servo-hydraulic actuators are a well-known type of actuator, and it would have been a matter of preference to the system designer to choose that particular type of actuator. These would have been an advantageous addition to the system disclosed by Antonov since it would have allowed the workstations to send data and instructions to processors connected to actuators to control devices connected to the system.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect actuators to at least one processor to allow instructions to be sent to that processor to control devices connected to the system through the actuator.

48. Claims 18, 43 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Antonov (US 5,884,046) in view of Grohn et al. (US 6,405,337).

49. With regard to claims 18, 43 and 44, while the system disclosed by Antonov shows substantial features of the claimed invention (discussed above), it fails to specifically disclose including a counter for determining a number of times said processed information is sent to said addressed processor, a sequencer for monitoring and controlling a testing operation as performed by said system, or limiting the number of times that said processed information can be sent from a sending processor.

Grohn teaches the use of a retransmission counter to count the number of times processed information is sent to a processor. Grohn further discloses a sequencer for monitoring and controlling a testing operation as performed by said system (current delays are compared to retransmission timeout) (Col 6, Line 62 to Col 7, Line 7). The current delays are compared with the retransmission timeout to determine when to decrement the counter. When the counter reaches zero, the communication line is assumed to have failed (Col 6, Lines 28-30 and Col 7, Lines 3-7). This causes the sending station to stop attempting retransmissions and allows error handling procedures to start.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a counter to count the number of times said processed information is sent to said addressed processor and use a sequencer for monitoring and controlling a testing operation as performed by said system. This would

have allowed error handling procedures to begin and stop the sending processor from attempting further retransmissions.

50. Claims 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Antonov (US 5,884,046) in view of Hillis (US 5,978,570).

51. With regard to claims 38-40, while the system disclosed by Antonov shows substantial features of the claimed invention (discussed above), it fails to specifically disclose the use of pointers for directing the flow of data between processors or directing a processor to a subsequent task to be performed.

Hillis teaches the use of pointers to direct a processor to a subsequent task to be performed and directing the flow of data between processors. Hillis discloses a task register holding a pointer to the next task and a next register holding a pointer to the next virtual processor in the list of virtual processors on the task (Col 14, Lines 65-67). The pointer is advanced through the list until an order has been executed for all processors in the list for that task (Col 14, Lines 24-27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use pointers for directing the flow of data between processors or directing a processor to a subsequent task to be performed since they allow a linked list of items in memory to be quickly traversed and executed.

52. Claims 9-13,28-32, 48-58, and 60-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Antonov (US 5,884,046) in view of Blumrich et al.

53. With regard to claims 9 and 28, while the system disclosed by Antonov shows substantial features of the claimed invention (discussed above), including that the first and second processors can address and forward processed information to each of the indexed processors within the system, it fails to specifically disclose creating a virtual memory map of each of the codes within each of the first and second processors for this purpose.

Blumrich teaches the use of virtual memory maps to map virtual memory locations to nodes in a distributed system. This allows messages to be sent to other nodes simply by addressing them to the virtual memory location, reducing overhead required to transfer data (Page 2, Section 2 and Page 6, Section 4.2). This would have been an advantageous addition to the system disclosed by Antonov since it greatly reduces the overhead of communication between nodes.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a virtual memory map as disclosed by Blumrich to contain addressing information for each of the processors in the system. This would have greatly reduces the overhead required for sending messages between the nodes in the system.

54. With regard to claims 10 and 30, Antonov further discloses that addressing the processed information is further defined as assigning a destination address onto the

processed information indicative of the code of the addressed processor (Packets identify the workstation they are intended for) (Col 5, Lines 49-53).

55. With regard to claims 11 and 31, Antonov further discloses storing the processed information within a memory location of the addressed processors. Since the message is received by the addressed processor (Col 5, Lines 63-65), it must be stored in a memory location at that processor.

56. With regard to claims 12 and 32, as discussed regarding claims 10 and 30, Antonov further discloses that addressing the processed information is further defined as assigning a memory address onto the processed information indicative of the memory location of the addressed processor (Packets identify the workstation they are intended for) (Col 5, Lines 49-53).

57. With regard to claim 13, Antonov further discloses stripping the destination address from sent processed information before the information is stored in the memory location. The addressing information used by Antonov is the MAC address of the communication interfaces (Col 5, Lines 41-44). When a MAC frame is received, the header containing the destination address is removed prior to passing the packet up to higher layers where it may be stored.

58. With regard to claim 29, Antonov further discloses that each of said first and second processors further include a hardware portion for assigning said first and second addresses to said first and second processed information, respectively. Antonov discloses that the workstations generate a data packet identifying another workstation to send the message to (Col 5, Lines 49-53). In order to generate the data packet identifying another workstation a hardware portion must be present in order to assign the correct address to the data and generate the packet.

59. With regard to claim 48, Antonov discloses a method of communicating across a distributed multiprocessing system having at least a first processor and a second processor (workstations) (Fig 2, 13), the first and second processors each having a memory location and being connected to each other by a communication link (Fig 1, 11, 11C, 17) said method comprising the steps of: indexing the first and second processors to define a different code for each of the processors for differentiating the processors; creating a virtual memory map of each of the codes within each of the first and second processors such that the first and second processors can address and forward processed information to each other; processing information within at least one of the first and second processors to define at least one of the first and second processors as a sending processor (Col 5, Lines 49-53); addressing the processed information to define at least one of the first and second processors as an addressed processor (Col 5, Lines 49-53); transmitting the processed information by utilizing the virtual memory map of the sending processor from the sending processor across the communication

link toward the addressed processor (inter-workstation message is routed to the recipient) (Col 5, Lines 55-65); receiving the processed information along with the address in the addressed processor; and storing the processed information within the memory location of the addressed processor (Col 5, Lines 63-65). Since the message is received by the addressed processor, it must be stored within a memory location of the addressed processor.

Antonov fails to specifically recite indexing the first and second processors to define a different code for each of the processors for differentiating the processors. However, in order for the processors to communicate with each other, they must be differentiated in order for messages to be routed to the intended recipient. Therefore, Antonov further discloses indexing the fist and second processors to define a different code for each of the processors for differentiating the processors, since the processors are able to identify and communicate with other processors (Col 5, Lines 49-51).

Antonov fails to specifically disclose creating a virtual memory map of each of the codes within each of the first and second processors such that the first and second processors can address and forward processed information to each other.

Blumrich teaches the use of virtual memory maps to map virtual memory locations to nodes in a distributed system. This allows messages to be sent to other nodes simply by addressing them to the virtual memory location, reducing overhead required to transfer data (Page 2, Section 2 and Page 6, Section 4.2). This would have been an advantageous addition to the system disclosed by Antonov since it greatly reduces the overhead of communication between nodes.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a virtual memory map as disclosed by Blumrich to contain addressing information for each of the processors in the system. This would have greatly reduces the overhead required for sending messages between the nodes in the system.

60. Claims 49-51 are rejected for the reasons cited above for claims 2-4, since they recite substantially identical subject matter.

61. Claim 52 is rejected for the reasons cited above for claims 5 and 6, since they recite substantially identical subject matter.

62. Claims 53,54,55,56,and 57 are rejected for the reasons cited above for claims 7,10,12,13, and 17, respectively, since they recite substantially identical subject matter.

63. With regard to claim 58, Anotov discloses a distributed multiprocessing system comprising; a first processor for processing information at a first station and for assigning a first address to a first processed information, a first memory location connected to said first processor for storing processed information, a second processor for processing information at a second station and for assigning a second address to a second processed information (workstations) (Fig 2, 13), a second memory location connected to said second processor for storing processed information, a communication

link interconnecting said first processor with said second processor for transmitting said first and second processed information between said first and second processors (Fig 1, 11, 17, 11C), defining at least one sending processor (message is received from sender at processing node)(Col 5, Lines 54-55), and said first and second memory locations storing received processed information to define at least one addressed processor (Col 5, Lines 63-65). Since the message is received by the addressed processor, it must be stored within a memory location of the addressed processor.

Antonov fails to specifically recite an indexer for indexing said first and second processors to define a different code for each of said processors for differentiating said processors. However, in order for the processors to communicate with each other, they must be differentiated in order for messages to be routed to the intended recipient. Therefore, Antonov further discloses an indexer for indexing the fist and second processors to define a different code for each of the processors for differentiating the processors, since the processors are able to identify and communicate with other processors (Col 5, Lines 49-51).

Antonov fails to specifically disclose that said first and second processors each including virtual memory maps of each code such that said first and second processors can address and forward processed information to each other.

Blumrich teaches the use of virtual memory maps to map virtual memory locations to nodes in a distributed system. This allows messages to be sent to other nodes simply by addressing them to the virtual memory location, reducing overhead required to transfer data (Page 2, Section 2 and Page 6, Section 4.2). This would have

been an advantageous addition to the system disclosed by Antonov since it greatly reduces the overhead of communication between nodes.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a virtual memory map as disclosed by Blumrich to contain addressing information for each of the processors in the system. This would have greatly reduces the overhead required for sending messages between the nodes in the system.

64. Claims 59,60,61,62,63,64,65,66, and 67 are rejected for the reasons cited for claims 23,29, 30, 32, 36, 37, 38, 39, and 40, respectively, since they recite substantially identical subject matter.

Conclusion

65. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

66. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron Strange whose telephone number is 571-272-3959. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glen Burgess can be reached on 571-272-3949. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS 12/9/2004

CLIFFORD A. BURGESS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100